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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,566	03/17/2004	Mou-Shiung Lin	985027-0109	3507

89518 7590 06/24/2010

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EXAMINER	
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ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
06/24/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

SIP_Docket@mwe.com

Office Action Summary	Application No.	Applicant(s)	
	10/802,566	LIN, MOU-SHIUNG	
	Examiner	Art Unit	
	AJAY K. ARORA	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,9-12,15,17-19,21,22,25,27,91,96-99,101-103,108-114 and 116-139* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/7/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1, 4, 7, 9-12, 15, 17-19, 21, 22, 25, 27, 29, 30, 91,96-99,101-103,108-115 and 116-139.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/10/2010 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7, 9-12, 15, 17-19, 21-22, 25, 27, 91, 96-99, 101-103, 108-114, 116-139 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 6,303,423), hereinafter Lin, in view of Nakanishi (US 6,921,980) of prior record, hereinafter Nakanishi.

Regarding claim 1, Lin (refer to Figures 1-2 and 10) teaches a circuit chip comprising:

a semiconductor substrate (10);

a transistor in and on said semiconductor substrate (Col. 7, lines 27-30);

multiple metal and dielectric (14, also see Col. 7, lines 36-39) layers over said semiconductor substrate;

a first contact pad (16 shown on left side of Figure 10) over said semiconductor substrate;

a passivation layer (18) over said multiple metal and dielectric layers (14), wherein a first opening in said passivation layer (18) is over a first contact point of said first contact pad (16 shown on left side of Figure 10) and said first contact point is at a bottom of said first opening (i.e. on bottom surface of first contact pad 16), wherein said passivation layer comprises a nitride (Col. 8, lines 52-56);

a second contact pad (16 shown on right side of Figure 10) over said semiconductor substrate;

a passivation layer (18) over said multiple metal and dielectric layers (14), wherein said passivation layer comprises a nitride (Col. 8, lines 52-56), wherein a first opening in said passivation layer (18) is over a first contact point of said first contact pad (16 shown on left side of Figure 10) and said first contact point is at a bottom of said first opening (i.e. on bottom surface of first contact pad 16), and wherein a second opening in said passivation layer (18) is over a second contact point of said second

contact pad (16 shown on right side of Figure 10) and aid second contact point is at a bottom (i.e. on bottom surface of second contact pad 16) of said second opening;

a power metal structure (structure directly above 16 shown on the right side, see Col. 8, lines 21-24) over said passivation layer (18) and on said first contact point, wherein said power metal structure is connected to said first contact point through said first opening (as first contact point is in the first opening and power metal structure is over the first opening), wherein said power metal structure comprises a metal layer;

a ground metal structure (structure directly above 16 shown on the left side, see Col. 8, lines 21-24) over said passivation layer (18) and on said second contact point, wherein said ground metal structure is connected to said second contact point through said second opening (as second contact point is in the second opening and ground metal structure is over the second opening), wherein said ground metal structure comprises a metal layer;

a capacitor (54) over said passivation layer (18), vertically over (but not necessarily directly over) said power and ground metal structures, and directly over said first contact point;

a first solder joint (joint corresponding to one of the 52) vertically over said first contact point and between a first terminal of said capacitor (first terminal of capacitor 54 that is just above first solder contact and which bonds with the first solder contact forming an electrical connection to the corresponding capacitor for input/output) and said power metal structure, wherein said first solder joint connects said first terminal to said power metal structure; and

a second solder joint (solder joint corresponding to the other of the 52) between a second terminal of said capacitor (second terminal of capacitor 54 that is just above second solder contact and which bonds with the second solder contact forming an electrical connection to the capacitor for input/output) and said ground metal structure, wherein said second solder joint connects said second terminal to said ground metal structure.

Lin does not teach that the metal layer of said power metal structure and said ground metal structure is a "copper layer" or that said power (and ground) metal structures each has a region used to be wirebonded thereto for connection made to a level of packaging. Nakanishi (refer to Figures 2a-2e and 3) teaches an integrated circuit with a semiconductor substrate (2) and a capacitor (8) mounted to a metallization structure comprising a copper layer (Col. 4, lines 58-63), which can server as a power or ground structure), wherein the metallization structure has a second region used to be wirebonded (by wirebonds 12) thereto for connection to next level of packaging (15). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin in view of Nakanishi so that said power metal structure and said ground metal structure has a first region and a second region, respectively, used to be wirebonded thereto for connection made to a next of packaging. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing routing for interconnects to contact pads that are closer to the periphery of the semiconductor substrate (compared to the capacitor, thus allowing flexibility of placing the capacitor in a central location on the semiconductor substrate,

as shown in Figure 3b of Nakanishi), while still being able to connect to the ground or power of next level of packaging without excessive wirebond length and a high electrical conductivity metal, like copper, which improves electrical performance and which allows long interconnect length, to connect to next level of packaging.

Regarding claim 7, Lin teaches substantially the claimed structure but does not teach that said ground metal structure further comprises "a gold layer" over said copper layer of said ground metal structure. Nakanishi teaches that copper metallization, which is usable as a ground metal structure, may further comprise a gold layer over said copper layer (Col, 4, lines 58-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that said ground metal structure further comprises a gold layer over said copper layer of said ground metal structure. The ordinary artisan would be motivated to modify Lin at least for the purpose of providing a layer that has increased resistance to corrosion.

Regarding claim 91, Lin teaches that said passivation layer (18) may comprise silicon nitride (Col. 7, lines 49-53).

Regarding claim 96, Lin teaches that said ground metal structure further comprises a nickel layer over said copper layer (Col. 9, lines 26-30) of said ground metal structure.

Regarding claim 97, Lin (refer to Figures 1-2 and 10) as modified in view of Nakanishi for claim 1, teaches a polymer layer (20 of Figure 10 of Lin) on said power and ground metal structures (as explained in rejection of claim 1), wherein a third opening (opening in 20 directly over 16 shown on right) in said polymer layer (20) is over a third contact point (point just above 16) of said power metal structure , and said third contact point is at a bottom of said third opening (as the point is just above 16), wherein a fourth opening in said polymer layer (opening in 20 directly over 16 shown on left) is over a fourth contact point of said ground metal structure, and said fourth contact point is at a bottom of said fourth opening (as the point is just above 16), wherein said first solder joint (solder joint corresponding to one of 52) is between said first terminal (first terminal of capacitor 54, as explained in rejection of claim 1) and said third contact point and connects said first terminal to said third contact point through said third opening (opening in 20 closest to 52), and said second solder joint (solder joint corresponding to other of 52) is between said second terminal (second terminal of capacitor 54, as explained in rejection of claim 1) and said fourth contact point, and connects said capacitor to said fourth contact point through said fourth opening (opening in 20 closest to 52).

Regarding claims 113 and 114, Lin (refer to Figures 1-2 and 10) teaches that said polymer layer (20) comprises polyimide, wherein said polymer layer has a thickness between 2 and 150 micrometers (Col. 8, lines 66-67 and Col. 7, lines 1-3).

Regarding claim 116, Lin teaches that said passivation layer (18) may further comprise an oxide (Col. 8, lines 54-56).

Regarding claim 117, Lin teaches substantially the claimed structure including that passivation layer comprises an oxide but does not teach that the passivation layer comprises silicon oxide. Nakanishi teaches that a passivation layer may comprise silicon oxide (Col. 4, lines 19-23). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin so that the passivation layer comprises silicon oxide. The ordinary artisan would have been motivated to modify Lin for at least the purpose of forming a passivation layer that has excellent moisture resistance and which is closely matched in coefficient of thermal expansion with silicon substrates.

Regarding claim 123, Lin (refer to Figures 1-2 and 10) as modified in view of Nakanishi for claim 1, teaches a polymer layer (20 of Figure 10 of Lin) on said power and ground metal structures (as explained in rejection of claim 1), wherein a third opening (opening in 20 directly over 16 shown on right) in said polymer layer (20) is over said first region, and said first region is at a bottom of said third opening (in polymer layer 20), and wherein a fourth opening (opening in 20 directly over 16 shown on left) in said polymer layer is over said second region, and said second region is at a bottom of said fourth opening.

The limitations of claims 124 and 125 have already been addressed in claims 113 and 114.

Regarding claim 126, Lin (refer to Figures 1-2 and 10) as modified in view of Nakanishi for claim 1, teaches a polymer layer (20 of Figure 10 of Lin) on said power and ground metal structures (as explained in rejection of claim 1), wherein a third opening (opening in 20 directly over 16 shown on right) in said polymer layer (20) is over a third contact point (point just above 16) of said power metal structure , and said third contact point is at a bottom of said third opening (as the point is just above 16), wherein a fourth opening in said polymer layer (opening in 20 directly over 16 shown on left) is over a fourth contact point of said ground metal structure, and said fourth contact point is at a bottom of said fourth opening (as the point is just above 16) wherein a fifth opening in said polymer layer (upper opening of 20 directly above third opening) is over said first region, and said first region is at a bottom of said fifth opening, and wherein a sixth opening in said polymer layer (upper opening of 20 directly above fourth opening) is over said second region, and said second region is at a bottom of said sixth opening, wherein said first solder joint (solder joint corresponding to one of 52) is between said first terminal (first terminal of capacitor 54, as explained in rejection of claim 1) and said third contact point and connects said first terminal to said third contact point through said third opening (opening in 20 closest to 52), and said second solder joint (solder joint corresponding to other of 52) is between said second terminal (second terminal of capacitor 54, as explained in rejection of claim 1) and said fourth contact point, and

connects said capacitor to said fourth contact point through said fourth opening (opening in 20 closest to 52).

The limitations of claims 127 and 128 have already been addressed in claims 113 and 114.

Regarding claim 9, Lin (refer to Figures 1-2 and 10) teaches an integrated circuit chip, comprising:

a semiconductor substrate (10);

a transistor in and on said semiconductor substrate (Col. 7, lines 27-30);

multiple metal and dielectric (14, also see Col. 7, lines 36-39) layers over said semiconductor substrate;

a first contact pad (16 shown on left side of Figure 10) over said semiconductor substrate;

a passivation layer (18) over said multiple metal and dielectric layers (14), wherein a first opening in said passivation layer (18) is over a first contact point of said first contact pad (16 shown on left side of Figure 10) and said first contact point is at a bottom of said first opening (i.e. on bottom surface of first contact pad 16), wherein said passivation layer comprises a nitride (Col. 8, lines 52-56);

a second contact pad (16 shown on right side of Figure 10) over said semiconductor substrate

a capacitor (54, also see Col. 14, lines 21-24) over said passivation layer (18) and over said second contact pad; and

a solder joint (solder joint corresponding to 52, also see Col. 14, lines 16-21) between a terminal of said capacitor (54), and said second contact pad, wherein said solder joint connects said terminal to said second contact pad; and

Lin does not teach "a third contact pad" wherein a contact area between said third contact pad and said second contact pad is horizontally offset from said first contact point". This limitation is similar to that addressed in claim 15.

Lin does not teach that the second contact pad is "connected to said first contact point through said opening, wherein the position of said second contact pad from a top perspective view is different from that of said first contact point, and wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer". Except for the last limitation, these limitations are similar to those already addressed in claims 15, 17 and 18. As for the thickness of first gold layer being "greater than 1 micrometer", the specific thickness of the gold layer is considered to involve routine optimization, which has been held to be within the level of ordinary skill in the art. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Lin such that said second contact pad comprises a gold layer with a thickness greater than 1 micrometer and there is an additional metal layer between said solder connection and said second contact pad. The ordinary artisan would be motivated to modify Lin at least for the purpose of providing a gold layer that

has optimal thickness for its intended purpose (such as providing resistance against corrosion, increasing wettability, etc.) for the given design and providing the additional metal layer to provide a barrier layer between the solder and the underlying device.

Note that the recitation "electroplated" in 3rd last line of claim 9 constitutes a product by process limitation in a product claim. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113. It is noted that applicant has not provided any evidence that applicant's invention requires a specific process (e.g. electroplating) to achieve a specific structure critical to the claimed invention. In the absence of the above, the product in the product-by-process claims is obvious from a product of the prior art (as stated above). For example, it would have been obvious to one of ordinary skills in the art at the time of the invention to utilize "electroplated" copper (instead of copper formed by another process) for at least the purpose of utilizing a known advantage of electroplated copper (for example, compared to electroless copper) such as greater suitability for achieving thicker coatings.

Regarding claims 10-11, the limitation of "a fourth contact pad over said semiconductor substrate" is similar to the "second contact pad" already addressed in view of Nakanishi

(note that Figure 3b of Nakanishi shows multiple wirebonded pads and they read on a second and third contact pad). The additional limitation that the third contact is used for wirebonding for "connection made to next level of packaging" has also earlier been addressed in view of Nakanishi. The limitation that "said second contact point is at a bottom of said second opening" is also similar to that addressed before.

Regarding claim 12, Lin (refer to Figures 1-2 and 10) as modified in view of Nakanishi teachs a fourth contact pad (16 in Figure 10 of Lin) over said semiconductor substrate (10), wherein a second opening in said passivation layer (18) is over a second contact point of said fourth contact pad (16), and said second contact point is at a bottom of said second opening. The claimed "fifth contact pad" on said second contact point is similar to the wirebonded pad of Nakanishi (as Nakanishi has multiple wirebonded pads, as described for claim 15; i.e. said fourth contact pad is used to be wirebonded thereto for connection made to next level of packaging.

Regarding claim 118, the limitation of a contact pad or metallization comprising a gold layer has already been addressed in 17. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin so that so that said fourth contact pad comprises a second gold layer. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing a second layer of high conductivity and corrosion resistance material to further improve corrosion resistance.

Regarding claim 98, the said capacitor (54) of Lin is capable of functioning a decoupling capacitor.

The limitations of claim 99 have already been addressed in claim 91.

Regarding claim 119, Lin (refer to Figures 1-2 and 10) as modified in view of Nakanishi for claim 1, teaches a polymer layer (20 of Figure 10 of Lin) over said passivation layer (18), wherein a second opening (opening in 20 directly over 16 shown on right) in said polymer layer (20) is over a second contact point (point just above 16) of said second contact pad (16 shown on right side of Figure 10), and said second contact point is at a bottom of said second opening (as the point is just above 16), and wherein said solder joint (corresponding to 50) is between said terminal (terminal of capacitor 54) and said second contact point (point just above 16) and connects said terminal to said second contact point through said second opening, wherein said third contact pad (pad corresponding to 50 of Figure 10) is between said solder joint and said second contact point.

The limitations of claim 120 have already been addressed in claims 113 and 114.

The limitations of claims 121 and 122 have already been addressed in claims 116 and 117.

Regarding claim 15, Lin (refer to Figures 1-2 and 10) teaches an integrated circuit chip, comprising:

a semiconductor substrate (10);

a transistor in and on said semiconductor substrate (Col. 7, lines 27-30);

multiple metal and dielectric (14, also see Col. 7, lines 36-39) layers over said semiconductor substrate;

a first contact pad (16 shown on left side of Figure 10) over said semiconductor substrate;

a passivation layer (18) over said multiple metal and dielectric layers (14), wherein said passivation layer comprises a nitride (Col. 8, lines 52-56), and wherein a first opening in said passivation layer (18) is over a first contact point of said first contact pad (16 shown on left side of Figure 10) and said first contact point is at a bottom of said first opening (i.e. on bottom surface of first contact pad 16);

a second contact pad (contact pad directly over first contact pad 16 which connects first contact pad to 50) over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening (in passivation layer 18);

a first polymer layer (20) over said passivation layer (18), wherein a second opening (opening in 20 through which 16 connects to 50) in said first polymer layer (20) is over a second contact point (contact point at surface of second contact pad that is nearest to 16) of said second contact pad, and said second contact point is at a bottom of said second opening;

a capacitor (54, also see Col. 14, lines 21-24) over said first polymer layer (20) and over said second contact point; and

a solder joint (joint corresponding to 52, also see Col. 14, lines 16-21) between said second contact point and a terminal of said capacitor (54), wherein said solder joint connects said terminal to said second contact point.

Lin does not teach the claimed third contact pad for wirebonding and its location, that "it is horizontally offset from said first contact point". Nakanishi (refer to Figures 2a-2e and 3) teaches an integrated circuit with a semiconductor substrate (2) and a capacitor (8) mounted to a first and second contact pad (contact pads to nearest to 8 to which 8 is connected), and a third contact pad (3 to which wirebond 12 is connected in Figure 3) over said semiconductor substrate (2), wherein said third contact pad is connected to first and second contact pads through an opening in the passivation layer (Col. 4, lines 19-23), wherein the position of said third contact pad (3) is horizontally offset from said first contact point (on first contact pad) and wherein said third contact pad has a region used to be wirebonded (to wirebond 12 of Figure 3b) thereto for connection made to a next level of packaging (15 of Figure 3b). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin in view of Nakanishi as above to include the claimed third contact pad for wirebonding and its location, such as the position of said third contact pad from a top perspective view is different from that of said first contact point. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing a third contact pad that is closer to the periphery of the semiconductor substrate compared to the capacitor (which allows flexibility of

placing the capacitor in a central location on the semiconductor substrate, as shown in Figure 3b of Nakanishi), while still being able to connect to the next level of packaging without excessive wirebond length.

Regarding claim 17, Lin teaches substantially the claimed structure but does not teach that said second contact comprises a "gold" layer. However, the use of a gold layer, such as a gold plating, over a contact metallization layer is well known in the art (see Nakanishi, Col, 4, lines 58-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that said second contact comprises a gold layer. The ordinary artisan would be motivated to modify Lin at least for the purpose of providing a layer that has excellent conductivity and resistance to corrosion.

Regarding claim 18, Lin teaches substantially the claimed structure but does not teach that said second contact comprises a "copper" layer. However, the use of copper for contact metallization is well known in the art (see Nakanishi, Col. 4, lines 58-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Lin so that said second contact comprises a copper layer. The ordinary artisan would be motivated to modify Lin at least for the purpose of using a high thermal and electrical conductivity metal for the second contact to minimize electrical losses and improved functionality.

Regarding claims 19 and 21, Lin as modified above in view of Nakanishi for claim 15, teaches a ground metal structure or a power metal structure (Col. 8, lines 21-23) connected to said capacitor (54 of Figure 10 of Line), to said wirebond (12 of Figure 3b of Nakanishi) and to said first contact pad (first contact pad 16 of Figure 10 of Lin).

Regarding claim 22, Lin (refer to Figures 1-2 and 10) teaches that said second contact point (as explained in rejection of claim 15) is further vertically over said passivation layer (18).

Regarding claim 25, Lin (refer to Figures 1-2 and 10) teaches that said passivation layer (18) may comprise silicon nitride (Col. 7, lines 49-53).

Regarding claim 27, Lin teaches substantially the claimed structure but does not teach that said third contact comprises "gold". The use of gold for a contact and its corresponding motivation has already been addressed in claim 7.

Regarding claim 101, the capacitor (54) of Lin (refer to Figures 1-2 and 10) is capable of functioning as a decoupling capacitor.

Regarding claim 102, Lin (refer to Figures 1-2 and 10), as modified in view of Nakanishi for claim 15, teaches a third opening in said first polymer layer is over said region of said third contact pad , and said region is at a bottom of said third opening. Note that

an opening in the first polymer layer is a necessary condition for wirebonding taught by Nakanishi.

Regarding claim 103, Lin (refer to Figures 1-2 and 10) teaches that the said first polymer layer (20) comprise polyimide (Col. 9, lines 4-5).

The limitations of claim 108 have already been addressed in claim 125.

Regarding claims 109 and 110, said first, second and third contact pads are configured to be capable of receiving ground voltage or power supply voltage.(Col. 8, lines 21-24).

The limitations of claims 111 and 112 have already been addressed in claims 116 and 117.

All limitations of claim 129 have been addressed in claims 9, except "a third contact pad between said solder contact and said second contact pad, wherein said third contact pad is finished with solder wettable material comprising gold". Lin (refer to Figure 10) also teaches a third contact pad (pad to which 52 is attached) between said solder contact (52) and said second contact pad, but does not specifically state that said third contact pad is "finished with solder wettable material comprising gold". However, given that this is a well known configuration in the art to improve solder wettability and 52 comprises solder, it would have been obvious to one of ordinary skills in the art at the

time of the invention to modify Lin so that said third contact pad is finished with solder wettable material comprising gold. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing a solder wettable coating that also provides good corrosion resistance prior to soldering.

Regarding claims 130 and 131, the "fourth contact pad" is the other wirebonded pad of Nakanishi which is also "used to be wirebonded thereto for connection to next level of packaging". It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin so that Lin includes the claimed "fourth contact pad over said semiconductor substrate" as claimed. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing a fourth pad near the periphery of the substrate which would provide a wirebond connection to the next level of packaging (15 of Nakanishi) without unduly long wirebonds (so that electrical performance is not degraded).

Claim 132 requires "fourth contact pad" and "fifth contact pad" which have a similar function of facilitating interconnection and providing wirebonding to next level of packaging as discussed above. It would have been obvious to one of ordinary skill in the art to use additional contact pads teaching of Nakanishi in Lin to create a structure, as claimed, because such structure is considered to be a duplication of parts that has no patentable significance unless a new unexpected result is produced. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960), MPEP 2144.04.

Claim 133 is similar to claim 118 and hence the same reasoning applies.

Claim 134 is similar to claim 98 and hence the same reasoning applies.

Claim 135 is similar to claim 25 and hence the same reasoning applies.

The limitations of claim 136 have already been addressed in claim 119.

The limitations of claim 137 have already been addressed in claim 125.

The limitations of claims 138 and 139 have already been addressed in claim117.

Response to Arguments

3. Applicant's other arguments filed 05/10/2010 regarding 35 U.S.C. 103 rejections of claims have been fully considered but they are not persuasive.

4. On pages 14-16, applicant argues about claim 1 saying that Lin's capacitor is not the same as applicant's capacitor because it is not "vertically over" a first contact point. This argument is not persuasive. First of all, vertically over is different from directly vertically over – vertically over simply suggest above. Further, it does not appear that applicant's capacitor electrodes are all directly over the said first point (see for example right electrode 23 of Figure 3 which is not directly over 16).

5. Applicant objects to use of Nakanishi as Nakanishi's terminals are connected to an external circuitry through the wiring traces 5 (see page 15, last para). However, it is noted that those are finally connected to the outside using the wirebonds; Nakanishi

teaches "a region used to be wirebonded thereto for connections made to next level of packaging". It is also noted that just because a part of an integrated circuit (such as capacitor 54 of Lin's Figure 10) is shown connected to an internal pad of a die (such as pad 16 of Figure 10 of Lin), it does not exclude the possibility of making other connections (including connections to external components) to the capacitor 54. How various components are interconnected depends on circuit design and the present claims do not recite any specific circuit details that would specifically not allow multiple connections to a component (such as interconnection with both an internal and external component), and neither has applicant provided any evidence in support of the above.
6.

7. Applicant's argument regarding claim 9 that "the present application is not identical to a metal having a combination of nickel and gold" (see page 17, 2nd para) is not persuasive. Applicant's claims only recite gold and hence Shirasaki is pertinent, whether or not other metals are present (as these are not excluded in the recited claims). Shirasaki teaches that a contact pad may comprise a first gold layer with a thickness that may be greater than 1 micrometer (see page 4, para 0052). Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin so that contact pad may comprise a first gold layer with a thickness that may be greater than 1 micrometer. The ordinary artisan would have been motivated to modify Lin for at least the purpose of optimizing the thickness to be suitable for a specific target corrosion resistance.

8. In response to applicant's argument that Arvin is nonanalogous art (see page 17), it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Arvin is also in the field of semiconductor electronic devices.

9. Additional arguments related to claim 15 not already addressed above are addressed by minor changes in rejection of claim 15 and associated explanations provided in the revised rejections. As such, those arguments are moot in view of the revised rejections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY K. ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on Mon through Fri, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Ajay K. Arora/
Examiner, Art Unit 2892